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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
BUR920030050US1
IBU-10-5757

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on November 1, 2006

Signature Carole Giacomazzo

Typed or printed name Carole Giacomazzo

Application Number	Filed
10/605,449	Sept. 30, 2003

First Named Inventor
Conti

Art Unit	Examiner
2829	J. M. Hollington

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 20,156
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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November 1, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of one forms are submitted.

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ARGUMENTS

It is the position of Applicants that the rejections of record are clearly not proper and are without basis for the following reasons:

The examiner has rejected claims 1-2 and 4-8 under 35 U.S.C. §102 (b) as being anticipated by Iino et al, U.S. Patent 5,568,054, hereinafter Iino et al. This rejection is not thought to be well taken for several reasons. Iino et al describe a technique to stop the testing of a defective device before excessive current causes damage. It is basically working like a circuit breaker or fuse. In the present application, the voltage is continuously varied to *each* device in order to obtain optimum burn in conditions for every device in the oven.

Iino et al do not monitor temperature or continuously vary voltage to maintain current at or below a set point. Such is taught and claimed in the present application. Iino et al do not have a burn in oven or a way to mount each chip individually (only the entire wafer as a whole). Moreover, in Iino et al, the power supply is turned off if an over voltage is detected. Since only one power supply 40 is shown (Col. 9, lines 25 and 26), apparently the power supply is shut off to every chip.

Col. 9, lines 26-29, does mention reducing voltage of power supply 40 instead of turning it off, but this is not described in detail. Since Iino et al disclose a single power supply 40, one would apparently be reducing voltage to all devices. In the present application, and as claimed, voltage is continuously controlled to *each chip* independently so *each* chip receives the optimal burn in voltage.

Turning now to the claims, method claims 1 and 2 and structural counterpart claims 7 and 8 each require at least one chip to be burned in and mounted individually in a tool having a device for mounting each chip individually, and a source of electrical current *individually* to burn in each chip, and a monitor to monitor the temperature of *each chip*. These limitations are not shown or taught in Iino et al. Also, claims 1, 2, 7 and 8 require monitoring at least current, or voltage or power levels, and varying the voltage to each chip to maintain at least one of the values below a given level. As explained above, Iino et al do not monitor temperature, or vary the voltage in response thereto to maintain one of the values measured below a given value. Iino et al merely turn off the power supply when an over current is detected. This is quite different from applicants' teaching and claims.

The examiner, in responding to applicants' arguments (page 2 of the final rejection), fails to recognize that the voltage is varied in response to either the current, voltage, or power input. There is no comparison, with a preselected current value above which it is turned off. Rather, the voltage is varied to maintain at least one input value below a given value. Moreover, the voltage in applicants' device is not switched off totally, and then restarted. The examiner also fails to note that the claims require that the chips be individually mounted.

Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

"Anticipation requires identity of the claimed process and a process of the prior art; the claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference" Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc. 45 F. 3d 1550, 1554, 33 USPQ2d 1496, 1498 (Fed. Cir. 1995).

A possibility or probability that features of the prior art contained in the disclosure of the prior art is not enough to establish anticipation. The same characteristics must be a "natural result flowing" from what is disclosed. (Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed Cir. 1991).

Since Iino et al clearly do not have any of the above enumerated features, claims 1, 2, 7 and 8 are clearly allowable.

Claims 3-5 and 9-10 are dependent upon claims 1 and 7, respectively, directly or indirectly, and for the same reasons are believed to be allowable.

With regard to claims 4 and 10, it is respectfully submitted that Iino et al do not show any monitoring of the chip temperature as indicated above. The element 41 cited by the examiner is a *current measuring element*, not a *temperature* measuring element (Col. 4, lines 59-61). Thus, for this additional reason, claims 4 and 10 are allowable.

The examiner has rejected claims 1, 4-7 and 10-12 under 35 U.S.C. 102(b) as anticipated by Hamilton, U.S. Patent 5,911,897, hereinafter Hamilton. This rejection is not thought to be well taken. The Hamilton patent is controlling power to the *heater* that is attached to the heat sink; it is not controlling the voltage or current to the *device or chip* that is being burned in, as is

taught and claimed herein. The heat sink and heater assembly are part of the burn in equipment, typically in practice attached to the burn in socket, burn in board or the oven. As stated in Hamilton:

> A temperature control system for high power burn-in of integrated circuit chips which includes an individual heat sink at each of the integrated circuit chips to dissipate heat generated by the integrated circuit. A heater for each chip is provided and is temperature controlled so that heat may be added by the heater as a function of the heat generated by the integrated circuit chip. A temperature sensor is provided in close thermal contact with the integrated circuit chip to sense the temperature of the integrated circuit chip. A closed loop temperature controller is used to vary the amount of current provided to the heater to maintain a desired range of temperature. Thermal contact between the temperature sensor and the integrated circuit chips is insured by utilizing a spring to urge the sensor toward the integrated circuit chip.

Thus, Hamilton is controlling the temperature at each chip by controlling the temperature at the heat sink. Applicants' invention involves varying the *voltage or current* applied to the chips, not the power to the heat sink. This is an entirely different concept from that of Hamilton. After burning in the chip, it is removed from the burn in equipment and shipped to the customer. Applicants acknowledged in the application that there are many known ways to control the temperature of a heat sink. The Hamilton patent is one way. Other prior art involves controlling air or fluid flow or temperature, or using thermoelectric devices. Thus, Hamilton has nothing to do with the present invention. Hence, further discussion of Hamilton is not believed to be warranted.

In view of the above, it is believed that each of the claims now in the application is distinguishable, one from the other, and over the prior art; therefore, reconsideration and allowance of the claims is respectfully requested.

Respectfully submitted,

Date: November 1, 2006

By: _____
William N. Hogg, Reg. No. 20,156
CUSTOMER NO. 26679

WNH:cg

CLAIMS PENDING IN APPLICATION SERIAL NO. 10/605,449

1. (Previously presented) A method of controlling the burning in of at least one I/C chip in a burn in tool, wherein said tool has a device for mounting each chip to be burned in, a power source to supply electrical current individually to burn in each chip, and a monitor for each chip to continuously monitor the temperature value of each chip, comprising the steps of:

continuously monitoring at least one electrical value input to each chip selected from the group of current, voltage and power, and varying the voltage to each chip to maintain at least one of the values at or below a given value.

2. (Previously presented) The method of claim 1 wherein the voltage at each chip is varied to maintain the current value below a given value.

3. (Previously presented) The method of claim 1 wherein the voltage at each chip is varied to maintain the power value below a given value.

4. (Previously presented) The method of claim 1 wherein each device temperature is monitored individually and the voltage to each device is individually varied to maintain the device at a given temperature.

5. (Previously presented) The method of claim 1 where there is a heat sink in contact with the chip.

6. (Previously presented) The method of claim 5 wherein the chip temperature of each chip is monitored and the temperature of the heat sink is varied to maintain the device temperature at a given value.

7. (Previously presented) A burn in tool for burning in at least one I/C chip comprising:

a structure for mounting each chip to be burned in individually;

a power source to supply electrical current individually to burn in each chip;

a structure for continuously monitoring at least one electrical value input to each chip individually selected from the group of current, voltage and power, and

a structure to vary the voltage to maintain at least one of the values of each chip at or below a given value.

8. (Previously presented) The tool of claim 7 wherein the voltage is varied to maintain the current value at each chip below a given value.

9 (Previously presented) The tool of claim 5 wherein the voltage is varied to maintain the power value at each chip below a given value.

10. (Previously presented) The tool of claim 7 including a monitor to continuously monitor the temperature value of each chip individually being burned in and wherein the voltage is varied to maintain the temperature value of each chip individually at a given value.

11. (Previously presented) The tool of claim 7 wherein a heat sink is in contact with each chip.

12. (Previously presented) The tool of claim 7 wherein the tool has a heat sink and temperature monitor for each chip and each heat sink has means to control the temperature of the heat sink, and the temperature control means is varied to maintain the temperature value of each chip at a given value.